Q.P. Code: **16EC5701** **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
M.Tech I Year I Semester (R16) Regular Examinations January 2017
VLSI TECHNOLOGY
(Common to ES & VLSI)
(For Students admitted in 2016 only)

Time: **3 hours** Max. Marks: **60**

(Answer all Five Units **5 X 12 =60** Marks)

UNIT-I

Q.1	a.	Explain about the Structure of NMOS transistor	7M
	b.	Compare NMOS and CMOS technology.	5M
		OR	
Q.2		Determine the Pull-up and Pull-down ratio of for NMOS inverter through one or more pass transistors.	12M

UNIT-II

Q.3	a.	What are layout design rules? Explain the layer representations and based design rules for CMOS process	8M
	b.	Discuss the wiring capacitances	4M
		OR	
Q.4	a.	Explain in detail about switch Logic and Alternative Logic.	6M
	b.	Briefly explain about Low Power Gates.	6M

UNIT-III

Q.5	a.	Explain briefly about power optimization of combinational logic network.	6M
	b.	Explain various simulators used for combinational logic?	6M
		OR	
Q.6	a.	Briefly explain the block diagram of phase locked loop for clock generation.	6M
	b.	Explain different simulators involved in validation process.	6M

UNIT-IV

Q.7		Explain Packages, I/O architectures and Pad design concepts in off chip.	12M
		OR	
Q.8	a.	Explain and compare ASAP and ASLP in data flow graphs	7M
	b.	Explain about linear feedback shift register.	5M

UNIT-V

Q.9	a.	Explain about logic synthesis.	7M
	b.	Explain scheduling and binding.	5M
		OR	
Q.10	a.	Explain about technology dependent logic optimization.	8M
	b.	Explain about global routing in layout synthesis.	4M

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